IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	Group Art Unit: 2644
Jing-Lu Gu	Examiner: L. Grier
Serial No.: 08/936,559	
Filed: September 24, 1997	
For: MULTIPLE FUNCTION, BI-DIRECTIONAL INPUT/OUTPUT INTERFACE FOR SOUND PROCESSING SYSTEM	San Francisco, California

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Colleen Bow

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P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF UNDER 37 C.F.R. 1.192

ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Gerald P. Parsons, Reg. No. 24,486
PARSONS HSUE & DE RUNTZ LLP
655 Montgomery Street, Suite 1800
San Francisco, California 94111
Telephone: (415) 318-1160
Facsimile: (415) 693-0194

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I. REAL PARTY IN INTEREST

The real party in interest is SanDisk Corporation, a corporation of the state of Delaware, the assignee of all right, title and interest in the present patent application from the inventor, Jing-Lu Gu.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

The subject application was filed on September 24, 1997, with original claims 1-24. The first Office Action on the merits (January 19, 2000) rejected all claims on prior art and claims 6 and 9 also under 35 U.S.C. 112, second paragraph, for insufficient antecedent basis. An Amendment (mailed May 19, 2000) in response to the first Office Action cancelled claims 1, 3, and 10; changed the dependence of claim 7; rewrote claims 2, 4, 8, and 11 in independent form, with further amendments in the case of claims 4 and 8; amended claims 6 and 9 to overcome the 35 U.S.C. 112, second paragraph, rejections; corrected a spelling error in claim 17; and added new claims 25-28. A second, final Office Action on the merits (August 26, 2000) upheld the previous rejections of all pending claims on prior art.

An Amendment (mailed on January 26, 2001) in response to the second, final Office Action, filed together with a Request for Continued Examination, added new claims 29-36, but left the previously pending claims unchanged. A third Office Action (April 11, 2001) introduced new grounds and rejected all pending claims. An Amendment (mailed August 10, 2001) in response to the third Office Action cancelled claims 2 and 13-16; rewrote claim 17 in independent form; and changed the dependence of claims 18 and 19. A fourth, non-final Office Action (October 24, 2001) indicated the allowable of claims 12, 22, and 28 if rewritten in independent form and introduced new grounds for the rejection of the other pending claims. An Amendment (mailed on January 24, 2002) in response to the fourth Office Action consequently rewrote claims 12, 22, and 28 in independent form and also amended claims 4, 8, 11, 20, and 34.

A fifth, final Office Action on the merits (May 23, 2003) allowed claims 12 and 28 and rejected all of the other pending claims on new grounds, including the withdrawal of the previously indicated allowability of claim 28. A Petition to Reconsider Finality (mailed June 3, 2003) was filed on the basis that the finality of fifth Office Action was improper as it rejected original claims on new grounds. A communication withdrawing the finality was mailed on July 21, 2003. A sixth, non-final Office Action (October 2, 2003) essentially reiterated the fifth Office Action, but without the finality.

A Response to the sixth, non-final Office Action contained no changes to the claims. A seventh, non-final Office Action on the merits (May 19, 2004) allowed claim 28 and rejected all of the other pending claims on new grounds, including the withdrawal of the previously indicated allowability of claim 12. A Notice of Appeal (August 19, 2004) was filed concurrently with an Amendment in response to the seventh, non-final Office Action, wherein claims 8, 9, and 29 were cancelled; claims 30 and 33 were rewritten in independent form; and claim 31 had its dependence changed.

In the course of preparing the present Appeal Brief, it was noticed that dependent claim 26, which was dependent on the previously cancelled claim 9, was not cancelled concurrently with claim 9. Consequently, an Amendment is being filed concurrently with the present Appeal Brief to rectify this inconsistency.

Claims 4-7, 11, 12, 17-25, 27, 28, and 30-36 are currently pending. Claim 28 has been allowed. Claims 4, 17, 30-31, 34 and 36 stand rejected under 35 U.S.C. §102(b) as anticipated by Henderson *et al.*, U.S. patent number 5,671,271. Claims 5-7, 11, 12, 18, 19, 20, 22-25, 27, and 32 stand rejected under 35 U.S.C. §103(a) with Henderson as the primary reference. No explicit reasons are given for the rejection of claims 21, 33 and 35.

IV. STATUS OF AMENDMENTS

An Amendment filed concurrently with the Notice of Appeal cancelled claims 8, 9, and 29, rewrote claims 30 and 33 in independent form, and changed the dependence of claim 31. An Amendment filed concurrently with the present Appeal Brief cancels claim 26. No other Amendments have been filed since the August 19, 2004, mailing date of the Notice Appeal.

V. SUMMARY OF THE INVENTION

The present invention relates to sound processing systems and particularly to systems and circuits having a multifunction analog input/output interface for connection to a speaker that handles input, output, and activation functions. Embodiments of the present invention provide a multifunction analog input/output interface with a low pin count and fewer components through the use of a speaker as both an output device (speaker) and as an input device (microphone). In particular, output circuitry drives the speaker in a conventional manner for sound output; and for sound input, sounds oscillate a speaker's diaphragm and magnet which induces an analog signal from the speaker that input circuitry amplifies. The number of system components for a record and playback system are thus reduced by eliminating the need for a separate microphone. Pin count is reduced since pins connected to the speaker are bi-directional to handle both input and output analog signals. Separate input pins for analog input signals and output pins for analog output signals are not required.

Another embodiment of the invention includes a system where an input signal from a speaker activates a system operation such as sound recording or playback. To activate the operation a user can touch the speaker or make a noise to cause the diaphragm to move. The movement of the speaker diaphragm generates an input signal that activates the system function, for example, by activating playback of a previously recorded signal. In the case of sound playback, a delay circuit disables reactivation of an operation until vibrations that a previous operation caused in the speaker have ceased. Using the interface for multiple functions in this manner further reduces pin count by eliminating a separate pin for controlling activation of the circuit's function. Additionally, the speaker serves multiple functions devices including the functions of a speaker, a microphone, and an activation switch in a conventional sound processing system.

In one embodiment, a playback system formed in an integrated circuit requires only three I/O pins, one for connection to a speaker, one for connection to a supply voltage, and one for connection to ground. This playback system can be package in a simple and inexpensive three-pin packages such as a T092 package.

VI. ISSUE

The Board is asked to review the correctness of the rejections under 35 U.S.C. §102(b) or §103(a). Specifically, claims 4, 17, 30-31, 34 and 36 stand rejected under 35 U.S.C. §102(b) as anticipated by Henderson *et al.*, U.S. patent number 5,671,271. Claims 5, 6, 25, and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Henderson in view of Bobry, U.S. patent number 5,593,236. Claims 11, 12, and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Henderson as the sole reference. Claim 32 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Henderson in view of applicant's admitted prior art. Claims 20, 22, and 23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Henderson in view of Willy, U.S. patent number 3,979,566. Claims 7, 18, and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Henderson in view of Thomson, U.S. patent number 5,452,274. No explicit reasons are given for the rejection of claims 21, 33 and 35. The issue is whether the Henderson patent either discloses the necessary elements to support a rejection under 35 U.S.C. §102(b) or, in the case of claims 11, 12, and 19, whether a rejection under 35 U.S.C. §103(a) as the sole reference is well founded.

VII. GROUPING OF THE CLAIMS

All of the claims stand rejected under 35 U.S.C. §102(b) or §103(a) and can be broken into three groups representing differing aspects of the present invention:

Group I: 4-7, 17-19, 20-25, 27, and 33-36.

Group II: 11, 12, and 19.

Group III: 30-36.

Independent claim 4 is suitable for deciding whether Group I of claims patentable; independent claim 11 is suitable for deciding whether Group II of claims patentable; and independent claim 30 is suitable for deciding whether Group III of claims patentable.

VIII. ARGUMENT

Group I

The claims of Group I can be represented by independent claim 4, which is drawn to an aspect of the present invention whereby the circuit begins to drive the speaker, which connected both the input and output circuits of the integrated circuit by the same terminal, in an output operation in response to an input signal form the same speaker exceeding a threshold level.. Claim 4 stands rejected under 35 U.S.C. §102(b) as anticipated by Henderson *et al.*, U.S. patent number 5,671,271. Claim 4 reads, in whole as:

> 4. A sound processing system comprising:
> a speaker;
> an integrated circuit having a first terminal coupled to the speaker, the integrated circuit further comprising:
> an output circuit coupled to the first terminal, wherein the output circuit applies to the first terminal an analog output signal to drive the speaker;
> an input circuit coupled to the first terminal, wherein the input circuit processes an input signal from the speaker via the first terminal
> a functional unit; and
> an activation circuit that activates the functional unit *in response to the input signal from the speaker exceeding a threshold level*, wherein the functional unit is coupled to the output circuit and *begins an output operation to drive the speaker in response to being activated by the activation circuit.*

The belief the rejection under 35 U.S.C. §102(b) is not well founded is based primarily on the last element, particularly the portions with the added emphasis.

In rejecting claim 4, the Office Action identifies cites column 15, lines 30-52, and Figure 5 of Henderson. As described in Henderson, Figure 5 shows a card or circuit board 550 having a power supply 553, a playback switch 556, a capacitor for memory retention 552, selection switch 554, an output transducer (speaker) 557, a sound input means 555, and an integrated circuit 551. Henderson describes this figure beginning at column 14, line 39. As noted in the Office Action, at lines 30-34 Henderson states that the sound output means 557 may also be used as the sound input means. Consequently, the Office Action is respectively identifying the elements 557 and 551 with the "speaker" and "integrated circuit" of the claim, in which case either of pins 3 or 4 of element 551 is identified with the "first terminal" of the claim.

However, as described at the cited location of column 15, lines 30-52, the elimination of the sound input means is described only in terms of a recording or *input* process, with no

indication of beginning an *output* operation as described in claim 4; further, to achieve this function requires the closure of programming switch 554 ("the sound input means can be activated *by closure of programming switch* 554 in which sound means 555 may be eliminated"[col.15, lns.30-32; emphasis added]), not in response to an input signal. It is believed that Henderson has not presentation of the use of a single speaker to supply input in order begin an output operation, as specified in claim 4. (The activation aspect, believed to be the main error in the Office Action, is described further below.)

Concerning the "integrated circuit" of the claim, to properly reject claim 4 under 35 U.S.C. §102(b) would require that Henderson recite the various elements of the integrated circuit of the claim (output circuit, input circuit, functional unit, activation circuit) as being contained in the integrated circuit 551 of Figure 5. Instead, Henderson only refers to element 551 as an "integrated circuit" without giving details as to its elements. (The Office Action does not explicitly identify the "integrated circuit" of the claim as 551 and is somewhat unclear as to whether it intends the "integrated circuit" to be 551 or the entirety of Figure 5 since it states that Henderson discloses "an integrated circuit that includes a speaker ...".

Although it is believed that a rejection of claim 4 under 35 U.S.C. §102(b) is not well founded for any of the above reasons, it is respectfully submitted that the Office Action's major error with respect to claim 4 concerns its final element:

> an activation circuit that activates the functional unit *in response to the input signal from the speaker exceeding a threshold level*, wherein the functional unit is coupled to the output circuit and *begins an output operation to drive the speaker in response to being activated by the activation circuit.* [emphasis added]

This elements states that, in response to an input signal *received from the speaker* exceeding a threshold, an output operation is begun through the same speaker. It is believed that not only is this not presented in Henderson, but, rather, Henderson teaches an entirely different procedure for activating playback.

With respect to this element, the Office Action states that the integrated circuit of Henderson is "indicative of a functional unit (col.15, lines 42-43), wherein based upon *whether a switch is closed or not* to indicate different levels of sound pressure, inherently indicates that the activation of the functional unit is based upon exceeding a threshold level of an input signal." As the

added emphasis shows, the Office Action is admitting the output process of Henderson is based on *whether a switch is closed or not*. This is described column 15, lines 50-52, of Henderson: "replays the stored sound data by sound output transducer [speaker] 557 ... *upon depression of playback switch 556*." As indicated by the added emphasis, to begin output, Henderson requires depression of output switch 556, which is quite distinct from speaker 557, as can be seen their in Figure 5. Henderson has no teachings of the functional unit being activated "*in response to the input signal from the speaker exceeding a threshold level*", as recited in claim 4. The input from this switch is not even received upon the "first terminal" by which the speaker is connected to the integrated circuit. Additionally, there appears to be no indication of this switch's open or closed state being "indicate different levels of sound pressure", as stated in the Office Action.

It should also be noted that by associating the "activation circuit" of the claim with the playback switch 556, the Office Action is referring to an element which is not even part of the integrated circuit 551, as is required to meet the limitations of the claim.

(Concerning the location in Henderson cited in the Office Action with respect to this element (col.15, lines 42-43), it is again noted that this is reference to a programming operation, not an output operation. As Henderson states at line 31, and as noted in the remarks above, the programming process also relies upon use of distinct switch for activation, in this case programming selection switch 554.)

For any these reasons, it is respectfully submitted that a rejection of claim 4 in particular, and more generally the rest of the claims in Group I, under 35 U.S.C. §102(b) based on Henderson is not well founded should be withdrawn.

Group II

Concerning the claims of Group II, these are drawn to the aspect of the present invention whereby features of the present invention are contained in an embodiment as a 3-pin package and can be represented by independent claim 11. Claim 11 stands rejected under 35 U.S.C. §103(a) based on Henderson *et al.*, U.S. patent number 5,671,271, as the sole reference. Claim 11 reads, in whole as:

> 11. A sound processing system comprising:

a speaker;

an integrated circuit having a first terminal coupled to the speaker, the integrated circuit further comprising:

an output circuit coupled to the first terminal, wherein the output circuit applies to the first terminal an analog output signal to drive the speaker; and

an input circuit coupled to the first terminal, wherein the input circuit processes an input signal from the speaker via the first terminal,

wherein the integrated circuit is in a three pin package including a first pin connected to the speaker and the first terminal of the integrated circuit, a second pin for connection to a power supply, and a third pin for connection to ground.

The belief the rejection under 35 U.S.C. §103(a) is not well founded is based primarily on the last element, particularly the portions with the added emphasis. (Additionally, as noted above with respect to 4, it is believed that does not explicitly disclose the actual elements recited as comprising the integrated circuit.)

In its rejection of claim 11, the Office Action admits that "Henderson fails to specifically disclose a three pin package as claimed." It then goes on to state that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Henderson by incorporating a three pin package ...". It is respectfully submitted that not only are improper assumptions, based upon hindsight gained from the present invention, being made as to what would be obvious, but, more importantly, Henderson specifically teaches away from a 3-pin embodiment.

As shown in Henderson's Figure 5, the integrated circuit 551 has ten pins, nine of which are assigned specific functions. As discussed above with respect to claim 4, Henderson does describe (beginning at column 15, line 30) that the output transducer 557 can also serve an input function, in which case the pins labeled 1 and 2 in Figure 5 would not be need; however, as again described with respect to claim 4 and made explicit at column 15, line 31, this reduction requires the use of switch 554, which is assigned two pins of 551. This leaves at least seven pins having explicitly stated functions that are required according to the teachings of Henderson.

Consequently, it is believed to be not only non-obvious, based on Henderson, but, rather, that Henderson teaches away from a 3-pin embodiment. At the least, this would require the elimination of a connection for switch 556 and both connections for switch 554, which Henderson states is needed in order to use pins 3 and 4 to serve both an input and output function. Further,

claim 11 enumerate the use of one pin of the 3-pin package for connection to ground, a connection not explicitly indicated for integrated circuit 551 and which would require an additional pin assignment.

For these reasons, it is respectfully submitted that a rejection of the claims of Group II under 35 U.S.C. §103(a) with Henderson as the sole reference is not well founded and should be withdrawn.

Additionally, it should be noted that in the last sentence of its Response to Arguments section on page 9, the Office Action states: "in respect to the input/output pin, in the independent claims, the language fails to explicitly limit the input/output to only a single pin." With respect to the claims of Group II, this statement is incorrect. Each of these claims explicitly recite that the integrated circuit is in a 3-pin package and then enumerate the specific connections of the pins. In addition to a power connection and a ground connection, the remaining pin (the *only* remaining pin) of the 3-pin package is for the first terminal, which serves the combined input output function. (Henderson explicitly shows two pins, 3 and 4, explicitly devoted to just the speaker 557.) The use of only a single pin for the input/output function is further reinforced in claims 12, which gives an explicit example (T092) of a 3-pin package, and claim 19, with the reinforcing "exactly" in its second line.

Group III

The claims of Group III can be represented by independent claim 30, which is drawn to an aspect of the present invention whereby the integrated circuit receives an signal over its input/output pin, which it stores in a non-volatile memory, and is then able to read from the non-volatile memory and output a representation of this same audio signal. Claim 30 stands rejected under 35 U.S.C. §102(b) as anticipated by Henderson *et al.*, U.S. patent number 5,671,271. Claim 30 reads, in whole as:

> 30. An integrated circuit comprising:
> an input/output pin;
> *a memory array*, wherein said memory array is *comprised of non-volatile memory cells*; and
> a sound processing circuit including:
> a write circuit coupled to the memory array and to the input/output

pin, wherein the write circuit performs an input operation that includes *writing to the memory array a series of values representing an audio signal received from the input/output pin*; and

a read circuit coupled to the memory array and to the input/output pin, wherein the read circuit performs an output operation that *includes reading from the memory array and supplying to the input/output pin a series of values representing said audio signal.*

The belief the rejection under 35 U.S.C. §102(b) is not well founded is based primarily on the portions with the added emphasis.

In its rejection of claim 30, the Office Action states "Henderson means of memory are indicative of non-volatile memory cells", but provides no details. The only disclosure Henderson gives with respect to Figure 5 of a "means of memory" appear to be that at column 15, lines 9-11. This states that the integrated circuit 551 is "connected to *discrete* components 552 necessary for circuit operation *such as a capacitor* for memory retention." The use of a capacitor as a means of memory clearly implies a *volatile* memory; further, if this passage is interpreted as meaning that the capacitor itself is used as a memory means (instead of used to maintain another volatile memory), it is not part of the integrated circuit, but rather a discrete element. In either case, it is respectfully submitted that the description is indicative of a volatile memory rather than a non-volatile memory as is specified in the claim.

Consequently, it is respectfully submitted that a rejection of claim 30 in particular, and more generally the rest of the claims in Group III, under 35 U.S.C. §102(b) based on Henderson is not well founded should be withdrawn.

IX. CONCLUSION

It is Applicant's position, as indicated above, that the assertions of the Office Action are incorrect. The subject matter of the claims is neither anticipated by nor unpatentable over the Henderson reference. Accordingly, the rejection of the application should be reversed and the present patent application passed to issue.

Respectfully submitted,

Gerald P. Parsons — Date 12/16/04

Reg. No. 24,486

PARSONS HSUE & DE RUNTZ LLP
655 Montgomery Street, Suite 1800
San Francisco, CA 94111
(415) 318-1160 (main)
(415) 318-1163 (direct)
(415) 693-0194 (fax)

Appendix A

CLAIMS PENDING IN APPLICATION SERIAL NO. 08/936,559

(Claims 1-3 have been cancelled.)

4. A sound processing system comprising:

a speaker;

an integrated circuit having a first terminal coupled to the speaker, the integrated circuit further comprising:

an output circuit coupled to the first terminal, wherein the output circuit applies to the first terminal an analog output signal to drive the speaker;

an input circuit coupled to the first terminal, wherein the input circuit processes an input signal from the speaker via the first terminal

a functional unit; and

an activation circuit that activates the functional unit in response to the input signal from the speaker exceeding a threshold level, wherein the functional unit is coupled to the output circuit and begins an output operation to drive the speaker in response to being activated by the activation circuit.

5. The system of claim 4, wherein:

the functional unit comprises a memory array and access circuitry capable of reading values from the memory array; and

the output circuit comprises a converter coupled to the access circuitry, wherein the converter converts a series of values read by the access circuitry into an analog signal that determines the output signal.

6. The system of claim 5, wherein the input circuit comprises:

an amplifier coupled to the first terminal;

a second converter coupled to the amplifier and the access circuitry, wherein the

second converter converts the input signal from the speaker into a series of values read that the access circuitry writes to the memory array.

7. The system of claim 4, wherein the activation circuit includes a delay element coupled to prevent activation of the functional unit during a period following completion of an operation of the functional unit.

(Claims 8-10 have been cancelled.)

11. A sound processing system comprising:

a speaker;

an integrated circuit having a first terminal coupled to the speaker, the integrated circuit further comprising:

an output circuit coupled to the first terminal, wherein the output circuit applies to the first terminal an analog output signal to drive the speaker; and

an input circuit coupled to the first terminal, wherein the input circuit processes an input signal from the speaker via the first terminal,

wherein the integrated circuit is in a three pin package including a first pin connected to the speaker and the first terminal of the integrated circuit, a second pin for connection to a power supply, and a third pin for connection to ground.

12. A sound processing system comprising:

a speaker;

an integrated circuit having a first terminal coupled to the speaker, the integrated circuit further comprising:

an output circuit coupled to the first terminal, wherein the output circuit applies to the first terminal an output signal to drive the speaker; and

an input circuit coupled to the first terminal, wherein the input circuit processes an input signal from the speaker via the first terminal,

wherein the integrated circuit is in a three pin package including a first pin connected to the speaker and the first terminal of the integrated circuit, a second pin for connection to a power supply, and a third pin for connection to ground, and wherein the three pin package is a T092 package.

(Claims 13-16 have been cancelled.)

17. An integrated circuit comprising:

an input/output pin;

a sound processing circuit;

an output circuit coupled to the input/output pin, wherein the output circuit applies to the input/output pin an output signal representing a sound;

an activation circuit coupled to the input/output pin and the functional unit, wherein in response to an input signal from the input/output pin, the activation circuit activates the sound processing circuit;

an input circuit coupled to the input/output pin, wherein the input circuit, when active, transfers the input signal received from the input/output pin to the sound processing circuit; and

a control circuit coupled to the sound processing circuit, wherein the control circuit selects an operation performed by the processing circuit when the activation circuit activates the sound processing circuit, and

wherein the sound processing circuit comprises:

a first functional unit that performs an output operation to generate a signal to the output circuit and a second functional unit that performs an input operation to processes the input signal from the input circuit;

a memory array;

a read circuit coupled to the memory array, wherein the read circuit is part of the first functional unit and the output operation includes reading from the memory array a series of values representing a sound; and

a write circuit coupled to the memory array, wherein the write circuit is part of

the second functional unit and the input operation includes writing to the memory array a series of values representing the input signal.

18. The integrated circuit of claim 17, wherein the activation circuit comprises a delay element coupled to prevent the activation circuit from activating the sound processing circuit during a delay period following completion of an operation by the sound processing circuit.

19. The integrated circuit of claim 17, further comprising a die and a three-pin package in which the die is mounted, the three-pin package having exactly three pins including the input/output, a pin for connection to a power supply, and a pin for connection to ground.

20. A method for operating a sound processing system, comprising:

connecting a terminal of a sound processing circuit to a speaker;

creating a vibration in the speaker that causes the speaker to generate an input signal to the terminal of the sound processing circuit;

activating a functional unit in the sound processing circuit in response to the input signal; and

in response to activating the functional unit, generating an analog output signal from the functional unit through the terminal to the speaker, wherein the output signal drives the speaker to produce a sound.

21. The method of claim 20, wherein creating the vibration comprises making a noise that causes a vibration in the speaker.

22. A method for operating a sound processing system, comprising:

connecting a terminal of a sound processing circuit to a speaker;

creating a vibration in the speaker that causes the speaker to generate an input signal to the terminal of the sound processing circuit, wherein creating the vibration comprises touching in the speaker;

activating a functional unit in the sound processing circuit in response to the input signal; and

in response to activating the functional unit, generating an output signal from the functional unit through the terminal to the speaker, wherein the output signal drives the speaker to produce a sound.

23. The method of claim 20, wherein the sound processing circuit is an integrated circuit and the terminal is a bi-direction input/output pin of the integrated circuit.

24. The method of claim 20, wherein generating the output signal comprises performing an output operation, and the method further comprising disabling activation of the functional unit during a delay time following the completion of the output operation.

25. The system of claim 6, wherein the output signal is derived from said series of values.

(Claim 26 had been cancelled.)

27. The integrated circuit of claim 17, wherein the output signal is derived from said series of values.

28. A method for operating a sound processing system, comprising:

connecting a terminal of a sound processing circuit to a speaker;

creating a vibration in the speaker that causes the speaker to generate an input signal to the terminal of the sound processing circuit;

activating a functional unit in the sound processing circuit in response to the input signal; and

in response to activating the functional unit, generating an output signal from the functional unit through the terminal to the speaker, wherein the output signal drives the speaker to

produce a sound; and

recording an audio input by said functional unit through the speaker prior to creating the vibration, wherein the output signal is derived from the audio input.

(Claim 29 had been cancelled.)

30. An integrated circuit comprising:

an input/output pin;

a memory array, wherein said memory array is comprised of non-volatile memory cells; and

a sound processing circuit including:

a write circuit coupled to the memory array and to the input/output pin, wherein the write circuit performs an input operation that includes writing to the memory array a series of values representing an audio signal received from the input/output pin; and

a read circuit coupled to the memory array and to the input/output pin, wherein the read circuit performs an output operation that includes reading from the memory array and supplying to the input/output pin a series of values representing said audio signal.

31. The integrated circuit of claim 30, wherein said series of values are analog values.

32. The integrated circuit of claim 30, wherein said memory array comprises a FLASH EEPROM memory.

33. An integrated circuit comprising:

an input/output pin;

a memory array;

a sound processing circuit including:

a write circuit coupled to the memory array and to the input/output pin, wherein the write circuit performs an input operation that includes writing to the memory

array a series of values representing an audio signal received from the input/output pin; and

a read circuit coupled to the memory array and to the input/output pin, wherein the read circuit performs an output operation that includes reading from the memory array and supplying to the input/output pin a series of values representing said audio signal; and

an activation circuit coupled to the input/output pin and to the sound processing circuit, wherein the sound processing circuit is activated by the activation circuit to supply said audio signal to the input/output pin in response to an input signal received from the input/output pin.

34. A method for operating a sound processing unit, comprising:

connecting a terminal of a sound processing circuit to a speaker;

recording by the sound processing circuit an audio input received through the speaker;

generating an input signal to the terminal of the sound processing circuit; and

in response to the input signal, supplying from the sound processing circuit through the terminal to the speaker an analog output signal derived from the audio input, wherein the output signal drives the speaker to produce a sound.

35. The method of claim 34, wherein said input signal is generated by creating a vibration in the speaker.

36. The method of claim 34, wherein the sound processing circuit is an integrated circuit and the terminal is a bi-directional input/output pin of the integrated circuit.